REMARKS

In the Office Action of September 1, 2004, the Examiner (1) objected to the drawings, (2) objected to the specification and (3) rejected claims 1-3, 7-11, 14, 15 and 19-21, which are all of the pending claims. Applicant will respond to the issues presented in the Office Action, in the order in which they were raised.

Drawings

The Examiner had objected to Figs. 5, 6, and 8 because the reference designators are not readable. However, on August 12, 2004, seven sheets of formal drawings were filed. It would appear that they were not in the file when the Examiner acted upon the application. The formal drawings should resolve the objection.

Figs. 6A and 8 are amended to conform their output terminal and signal labels.

In addition, Fig. 9 has been added to show the embodiment of claim 3. As claim 3 and comparable text in the summary are part of the original disclosure, there is no new matter introduced by adding Fig. 9.

Specification

The Examiner has made various objections to the specification, each of which will be addressed.

First, the Examiner objected that the disclosure at page 7, lines 15-18, was confusing. That disclosure states that "the termination elements are coupled to the mid-point termination voltage." The Examiner contends or assumes that such disclosure refers only to Figs. 5 and 6 and that those drawings should show the termination elements being coupled to the mid-point termination voltage. Applicant assumes from the tenor of the Examiner's statement that he interprets the specification language to require that the termination elements be *directly* connected to the mid-point termination voltage. The Examiner is in error for two reasons. First, there is no requirement that every figure of the drawings show every feature of the invention. Thus, Figs. 5 and 6 are not intended to show every feature of the invention. Fig. 7 also requires consideration. Second, the language "coupled to" does not require a direct connection. One

skilled in the art would understand "coupled to" to permit indirect connections via intervening elements. Several Federal Circuit cases have confirmed this point.

The best point of reference for the quoted language on page 7 is not just Figs. 5 and 6, but also Fig. 7. When Fig. 7 is included, it will be seen that the termination elements 53 and 54 are connected to outputs outp and outn and that those outputs are, indeed, under the specified conditions, "coupled to" the mid-point termination voltage vmid (also written as "Vmid") as further explained below.

With reference to pages 13 and 14, we note first the statement on page 14, in the paragraph spanning lines 6 -11, that the switched current feedback amplifier Pamp4 of Fig. 6 (further illustrated in the example circuit of Fig. 8) is similar to the Fig. 7 amplifier. We further refer to the discussion of Fig. 7 amplifier Pamp2 on page 13. There, it is explained from lines 24-35 how vmid couples to the termination elements. Indeed, the relationship between the voltage on the input terminals and vmid determines whether current flows in the input terminals. If so, this signal current is converted to a voltage gain which drives the current at outp flowing from vcc to outp. Or, with the reverse polarity, when the input Inp is below vmid, then the current flowing in transistor mp1 is the current Imn9 minus the signal current. After signal current is converted to a voltage gain, that voltage drives the output device to reduce the current flowing from outp to ground. The mid-point termination voltage is thereby coupled to the termination elements which receive the output. The coupling is fully shown in Figs. 7 and 8.

To further expound, the signal path is differential. Vmid is a voltage reference input. Starting from that reference input, the voltage at the gates of transistors mn1, mn3 and mn5 is equal to Vmid + Vgsmn5 (where Vgsx is the gate-to-source voltage of transistor x). From the specification at page 13, line 7, transistor mp7 will conduct some known current. (Note that mp7 apparently is a depletion mode device.) This known current from transistor mp7 flows in the diode-connected transistor mn5 and thus sets the value of Vgsmn5. Similarly, transistor mn10 establishes a current in transistor mp5 and that current, in turn, sets a voltage at the gates of transistors mp1, mp3 and mp5, equal to Vmid - Vgsmp5. If input inp is at a voltage equal to reference Vmid, then transistor mn1 will have a gate-to-source voltage (Vgs) equal to the gate-to-source voltage of transistor mn5, and transistor mp1 will have a Vgs equal to the Vgs of mp5.

This means that transistor mn1 will conduct a current equal to the current in transistor mn5 and transistor mp1 will conduct a current equal to the current in transistor mp5. Likewise, transistor mp6 will conduct a current equal to that of transistor mp7, and transistor mn9 makes a current equal to that of transistor mn10. So, the currents from transistors mp6 and mn1 balance and the voltage at the gate of transistor mp2 can stay at its initial point. Similarly, the current from transistors mn9 and mp1 balance and the voltage at the gate of transistor mn2 can stay at its initial point. If the voltage input inp is lower than the voltage Vmid, then transistor mn1 turns on harder, pulling down on the gate of transistor mp2. This turns on device mp2 and pulls up on the output outp; also, transistor mp1 turns off and transistor mn9 can pull down on the gate of transistor mn2, turning off transistor mn2 and allowing the output outp to be pulled up by transistor mp2.

That is how the mid-point termination voltage couples to the termination elements.

Next, the Examiner indicates that he finds misleading the statement on page 8 that "while the voltage source maintains the second pair of terminals of the termination network at a pre-determined, non-zero potential. The predetermined, non-zero potential preferably comprises one-half of the line driver circuit supply voltage." The Examiner further expounds that in Fig. 7, there does not appear to be a connection between vmid and the voltage applied to the second pair of terminals of the termination network. As just indicated, however, this is an incorrect conclusion. There is a relationship between the voltage vmid and the voltage applied to the second pair of terminals of the termination network. The voltage vmid controls the magnitude of the input signal current and, consequently, controls the voltage applied to the second pair of terminals. The Examiner's objection is therefore unfounded.

To expand somewhat, if the voltage vp is higher than the voltage Vmid, then resistor r7 (Fig. 6A) pulls up on the input inp and turns off transistor mn1, allowing transistor mp6 to pull up on the gate of transistor mp2. This turns off transistor mp2, allowing transistor mn2 to pull down on the terminal vp. This negative feedback stops when the voltage on terminal vp equals vmid. A mirror image operation occurs with respect to the voltage on terminal vn.

Next, the Examiner objects to the statement on page 6, lines 23-28, that " In one aspect of the invention, the switching means comprises a first input for enabling and disabling the first

driving means and a second input for enabling and disabling the second driving means, wherein, when one of the first or second driving means is enabled, the other driving means is disabled." The Examiner asserts that this language is misleading because (1) there is no switching means, first input or second input shown in Figs. 5 or 6 and (2) there is only one "enable" signal shown in Figs. 5 and 6, applied to the first driving means (52). According to the Examiner "the second driving means (51) is always in the ON condition and has no enable/disable input ."

In response to the first point, the specification is amended to conform to the previous amendment of the claims, wherein "switching means" was changed to "control signal." Support for the change was previously discussed in connection with the amendments to the claims.

As to the Examiner's second point, reconsideration is requested as the Examiner has misconstrued both the text and the operation of the second driving means. The text does not state that the second driving means is turned "OFF" but, rather, that it is "disabled." Those are two different things! It is correct to state that the second driving means is disabled even though it does not receive the "enable" signal. It does not drive the line, so it is disabled. As explained on pages 10 and 11, in the case of Fast Ethernet, the bridge currents I1-I4 are turned OFF and the line is voltage driven from vp and vn. In the case of Ethernet, by contrast, nodes Vp and vn are set to an active mid-point termination voltage, vmid. The line is then driven from the bridge currents. That is, setting vp and vn to vmid effectively (i.e., operatively) disables the second driving means.

Reconsideration is therefore requested. No amendment is required.

Claim rejections - 35 USC §112

Claims 1 and 21 have been rejected under 35 USC 112, first paragraph, as not being based on an enabling disclosure. The Office Action asserts, with respect to claim 21, that the recitation "wherein the driver circuit operates to limit a voltage at the output to about one-half of the supply voltage" is not described in the specification; and he further asserts, with respect to claim 21, that the comparable recitation "limiting the output voltage to about one-half of a supply voltage for the driver circuit" is not described in the specification.

The Office Action is incorrect. Page 6, line 34-page 7, line 1 clearly discloses "wherein the driver circuit operates to limit the output voltage to about one-half of the supply voltage." Page 7, lines 15-23 recite, with respect to another aspect of the invention, "when the bridge current driver is selected, the terminating elements are coupled to the mid-point termination voltage and the lines are driven from the bridge current driver. When the voltage driver is selected, the bridge current driver is disabled, and the terminating elements are coupled to the voltage driver. Preferably, the mid-point termination voltage is approximately equal to one-half the supply voltage." Page 8 further discloses, at lines 8-17, driving the first pair of terminals with the current source while the voltage source maintains the second pair of terminals at a pre-determined, non-zero potential, which "preferably comprises one-half of the line driver circuit supply voltage." On page 13, at lines 12-14, referring to Fig. 7, it is explained that "the amplifier signals are referenced to half the power supply voltage, Vmid = 1.65V." Consequently, the disclosure makes quite clear that the output voltage of the driver circuit is limited to approximately the value Vmid. Use of the circuits of Figs. 7 and 8 will clearly provide the claimed operation, satisfying the enablement requirement.

Claim 11 also is rejected for lack of enablement. According to the Office Action "In this instance, the specification fails to explain how the voltage source maintains the second pair of terminals of the termination network at pre-determined, non-zero potential comprising one-half of line driver circuit supply voltage." The rejection is clearly erroneous. Sufficient passages have already been recited which establish that the second pair of terminals is maintained at a predetermined, non-zero potential and that that potential comprises one-half of the line driver circuit supply voltage (see, e.g., page 11, lines 1-4 "in the case of Ethernet, the vp and vn

voltages are set to an active mid-point termination voltage, vmid. Vmid is half the supply voltage or 1.65 V for a 3.3 V supply.") The claim limitation is therefore clearly taught and enabled.

Since operative circuits are disclosed in Figs. 7 and 8 and it was expressly stated that the mid-point termination voltage is set to half the supply voltage, there can be no question of enablement of any of the above-discussed claims. Whether the operation of the circuit is presented in sufficient detail for the Examiner or not, an operative circuit is disclosed and would be understood by those skilled in the art, meaning that the mere disclosure of such circuit by itself constitutes an enabling disclosure. Consequently, the foregoing rejections should be withdrawn.

Claims 1-3, 7-11, 14, 15, 19 and 20 were also rejected under 35 USC 112, second paragraph, for indefiniteness.

With respect to claims 1 and 2, the Examiner rejects as indefinite the recitation "at least one control signal for selecting between the first and second driving means" as the Examiner believes the recitation to be misdescriptive. The Examiner is correct that there is only one "enable" signal as applied to driving means 52 for enabling or disabling it. He is also correct that the second driving means (51) has no control signal applied to it, per se. He concludes, therefore, that the second driving means cannot be selected. That is where he goes wrong. The conclusion is totally unwarranted and incorrect. While the enable signal does enable and disable the first driving means, it also selects between the first and second driving means in doing so, rendering one enabled and the other disabled. The line is driven by only one of the first or second driving means at any time, in either Ethernet or Fast Ethernet mode. Consequently, the control signal does effect a selection of mode and a selection of driving means. Applicant can think of no more apt wording for this structure and operation. It is not misdescriptive. The Examiner is requested to review, reconsider, and withdraw the rejection.

Regarding claim 3, the Examiner objects to, as indefinite due to misdescriptiveness, the recitation "a logic control input signal enabling and disabling the first driving means; and a logical complement of the logic control signal for enabling and disabling the second driving means." He asserts that Figs. 5 or 6 or 6A show only one control signal applied to the first

driving device (51) and that they do not show a logic complement. Applicant has reviewed the specification and has amended claim 3 to be more consistent with the original wording of the claim. Applicant also has added a Fig. 9 to show the embodiment set forth in claim 3. As claim 3 and comparable text in the summary constitute parts of the original disclosure, there is no new matter introduced by adding Fig. 9.

Claim 8 is rejected because a recitation similar to that used in claims 1 and 2 has been deemed indefinite and misdescriptive. The recitation states "at least one control signal for selecting between the bridge current driver and the voltage driver, such that, when the bridge current driver is selected, the terminating elements are coupled to the mid-point termination voltage and the lines are driven from the bridge current driver; and when the voltage driver is selected, the bridge current driver is disabled and the terminating elements are coupled to the voltage driver." The Office Action states that only the bridge current driver (52) is enabled/disabled; that voltage driver 51 cannot be selected because there is no selecting signal applied to the voltage driver and that the terminating elements 53 and 54 are connected to the outputs of the elements 51 and 52, not to the voltage Vmid as recited. All of these points were raised and addressed above. They are all incorrect. The claim language is clear, definite, properly descriptive and fully enabled. Reconsideration and withdrawal of the rejection are requested.

With respect to claim 11, the language "wherein the line driver circuit...one-half of the line driver supply voltage" on lines 5-10 was held indefinite as being misdescriptive. According to the Office Action, there are no first and second modes of operation because Fig. 5 or 6 shows that the voltage source 51 is constantly "ON." As stated above with respect to claims 1 and 2, the Office Action indicates that no control signal was seen applied to the source 51. Further, it was not clear to the Examiner what the "non-zero potential" was meant to mean and how the voltage source 51 could maintain the "second pair of terminals of the termination network" at a non-zero potential which is one-half of the line driver circuit voltage. These points have all been discussed above. Had the Examiner reviewed all of Figs. 5-8 instead of just Figs. 5 and 6, he would have seen that the totality of the claim is fully disclosed and properly described in the claim. Reconsideration and withdrawal of the rejection are requested.

Regarding claim 14, the Office Action states there is a limitation which is indefinite and misdescriptive: "wherein the first mode of operation comprises voltage source drive mode." According to the Office Action, and referring to Figs. 5 and 6, the voltage source 51 cannot be selected because the voltage source 51 receives no mode control signal. The Office Action manifestly is incorrect.

The fact that the voltage source 51 receives no mode control signal does not mean that it cannot be selected; but, even beyond that, claim 11 does not speak in terms of "selecting" the voltage source. Rather, it states that the line driver circuit "operates in a first configuration to establish a first mode of operation, and in a second configuration to establish a second mode of operation" and it further states that the second mode of operation comprises a current source drive mode. In the current source drive mode, the first pair of terminals is driven with the current sources while the voltage source maintains the second pair of terminals at a predetermined, non-zero potential. This is clearly properly descriptive. The Examiner presents the claim language and the operation of the circuit in an unfair and incorrect light. He mischaracterizes the claim language and rejects claim language not in the claim. No "selection" is claimed. The rejection amounts to setting up a straw man and knocking him down. Reconsideration and withdrawal of the Office Action are requested.

Turning to claim 15, such claim is rejected as indefinite due to misdescriptiveness. Manifestly, this is erroneous. The claim is properly definite and clearly properly descriptive. In the rejection, it is stated that voltage source 51 is always activated during both the first and second modes. Nothing in the claim states otherwise. See the discussion of claims 11 and 14, above.

In claim 15, the recitation "the first configuration" is stated to lack antecedent basis. Clearly, this is inaccurate because claim 15 depends from claim 14 which, in turn, depends from claim 11; and claim 11 states in line 5 "the line driver operates in a first configuration to establish ..." . There is, thus, an express antecedent provided in claim 11.

The rejection of claim 15 should be reconsidered and withdrawn for each of these reasons.

Turning to claim 21, the Office Action rejects the claim due to indefiniteness in multiple recitations. First, it is stated that "the first mode of operation" and "the second mode of operation" are indefinite" because it is not clear how the two modes of operation can be selected." This is an improper rejection. The claim does not have to make it clear how the two modes of operation can be selected. The claim states, clearly and definitely, what happens when each of the modes of operation is selected. That is all that is required of the claim. The Examiner can point to no reason that the claim should have to state how the modes of operation are selected. Teaching how to select the modes of operation is the job of the specification, not the claim.

Claim 21 is further deemed indefinite because "limiting the output voltage to about one-half of a supply voltage for the driver circuit" is considered indefinite because "it is not clear ***how*** the output voltage can be limited to about one-half of a supply voltage." (Emphasis added.) Again, this is also an improper rejection because the claims need not make it clear how the output voltage can be limited. That is not an appropriate requirement for the steps of a method claim. The specification teaches how this is accomplished and that is all that is required. This rejection is legally unsupportable and should be withdrawn.

Claims 7, 9, 10, 19 and 20 have been rejected under 35 USC 112, second paragraph, based on the "technical deficiencies" of claims 1, 8 and 11. Applicant having fully addressed and overcome each of the rejections of claims 1, 8 and 11, the rejection of dependent claims 7, 9, 10, 19 and 20 now should be withdrawn.

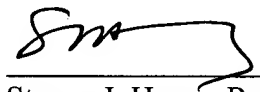
Applicant appreciates that the operation of the circuits of Figs. 6-8 may not be easy to understand and they may not be familiar kinds of circuits to the Examiner. However, Applicant has taken pains to assure that the driver circuit is accurately shown and described and has taken care to use language in the claims that is properly descriptive. It may be confusing to the Examiner that a single enable signal applied to a single driver can effect which of two drivers is "active," but that is precisely what is disclosed. The state of the Ethernet current driver determines the state of the Fast Ethernet voltage driver. The claim language is not misdescriptive. It is not unclear. It is entirely proper. Applicant requests reconsideration and withdrawal of all rejections and objections.

CONCLUSION

For each of the foregoing reasons, the rejections have now been fully overcome and the application is in condition for allowance. If the Examiner has any reservations, still, Applicant reiterates Applicant's previously stated willingness to arrange a telephone conference call to discuss with the Examiner to the Examiner's satisfaction the operation of Applicant's circuit in order to facilitate examination.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

By: 

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Date: December 23, 2004
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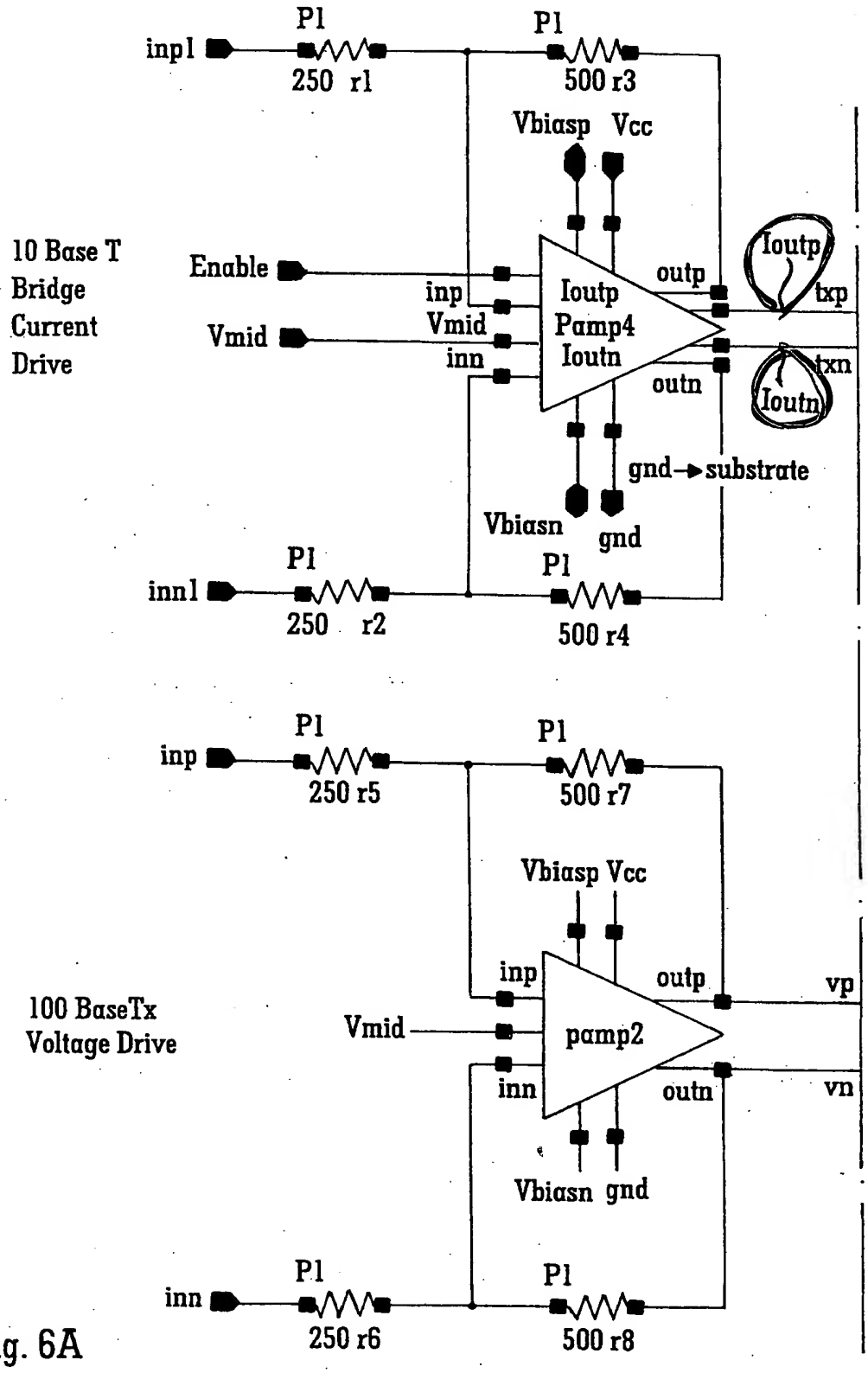
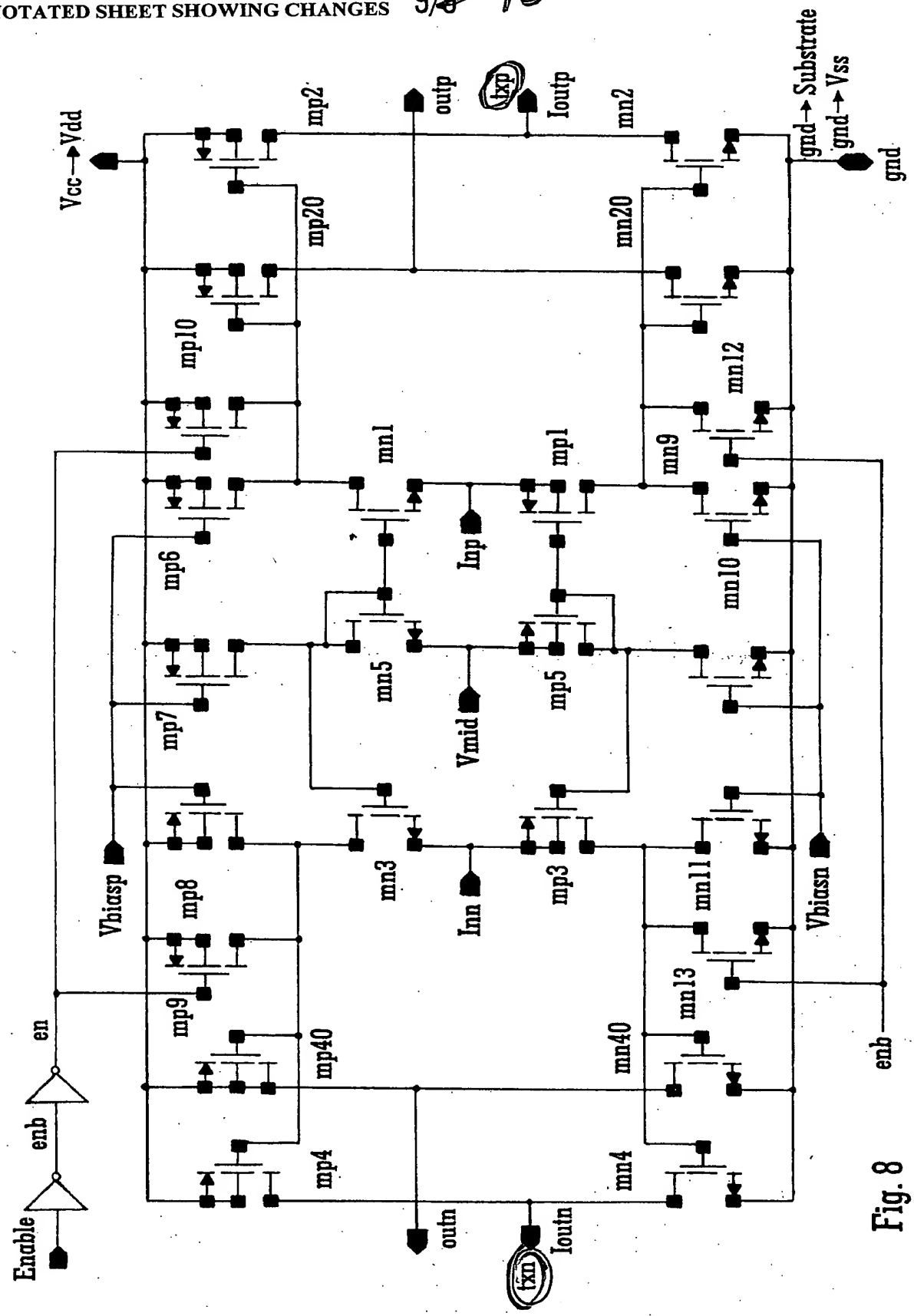


Fig. 6A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mp2
outp
Ioutp
mn2
gnd→Substrate
gnd→Vss
gnd
mp20
mn20
mp10
mn12
mn1
mp1
mn9
Inp
mp6
mn10
mn5
mp5
mp7
Vmid
Vbiasp
mp8
mn3
mp3
Inn
mn11
Vbiasn
mp9
mn13
en
mp40
mn40
enb
enb
mp4
mn4
Enable
outn
Ioutn
Ixp
Ixn

Fig. 8

In the Drawings

Applicant has added a new drawing figure, Fig. 9, to show the embodiment set forth in claim 3.

Applicant has also amended Figs. 6A and 8 to make consistent the labeling of outputs of Pamp 4. Copies of those figures marked in red and labeled "Annotated Sheet Showing Changes" are attached, along with Replacement Sheets for Figs. 1-8 and a new sheet for Fig. 9.